American International University- Bangladesh (AIUB) Faculty of Engineering (FE)

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| --- | --- | --- |
| Course Name : | Digital Logic and Circuit | Course Code : |
| Semester : | 05 | Sec : L |
| Lab Instructor : | MD. ALOMGIR KABIR |  |

Experiment No : 06

Experiment Name : Construction of MOSFET Logic Gates

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| --- | --- | --- | --- | --- |
| Submitted by (NAME): | Siam Tahsin Apon | | Student ID: | 22-49812-3 |
| Group Members | ID  1. | 22-49812-3 | Name  Siam Tahsin Apon | |
|  | 2. | 22-49822-3 |  | Md. Jubayar Hasan Emon |
|  | 3. | 22-49813-3 |  | Samrat Alam |
|  | 4. | 22-49806-3 |  | Shehab Ahmed |
|  | 5. | 22-49801-3 |  | Sheikh Zahidul Islam |
|  | 6. |  |  |  |
|  | 7. |  |  |  |
| Performance Date : | 28.03.2024 |  | Due Date : | 02.05.2024 |

Marking Rubrics (to be filled by Lab Instructor)

Marks

Category Proficient

[6]

Good [4]

Acceptable [2]

Unacceptable [1] Secured

Theoretical

All information,

All Information

Most information

Much information

Background, Methods

measures and variables provided that is

correct, but some

missing and/or

& procedures sections

are provided and explained.

All of the criteria are

sufficient, but more explanation is needed.

Most criteria are met,

information may be missing or inaccurate.

Experimental results

inaccurate.

Experimental results

met; results are

but there may be some don’t match exactly

Results

described clearly and accurately;

lack of clarity and/or incorrect information.

with the theoretical values and/or analysis is unclear.

are missing or incorrect;

Demonstrates thorough Hypotheses are clearly

Conclusions don’t

and sophisticated

stated, but some

Some hypotheses

match hypotheses, not

Discussion

understanding.

concluding statements missing or misstated;

supported by data; no

Conclusions drawn are appropriate for analyses;

Title page, placement of figures and figure

not supported by data or data not well integrated.

Minor errors in

conclusions not supported by data.

Major errors and/or

integration of data from different sources.

General formatting

captions, and other formatting issues all correct.

Writing is strong and easy to understand; ideas are fully

formatting.

Writing is clear and

easy to understand; ideas are connected;

missing information. Not proper style in text.

Most of the required criteria are met, but

Writing & organization

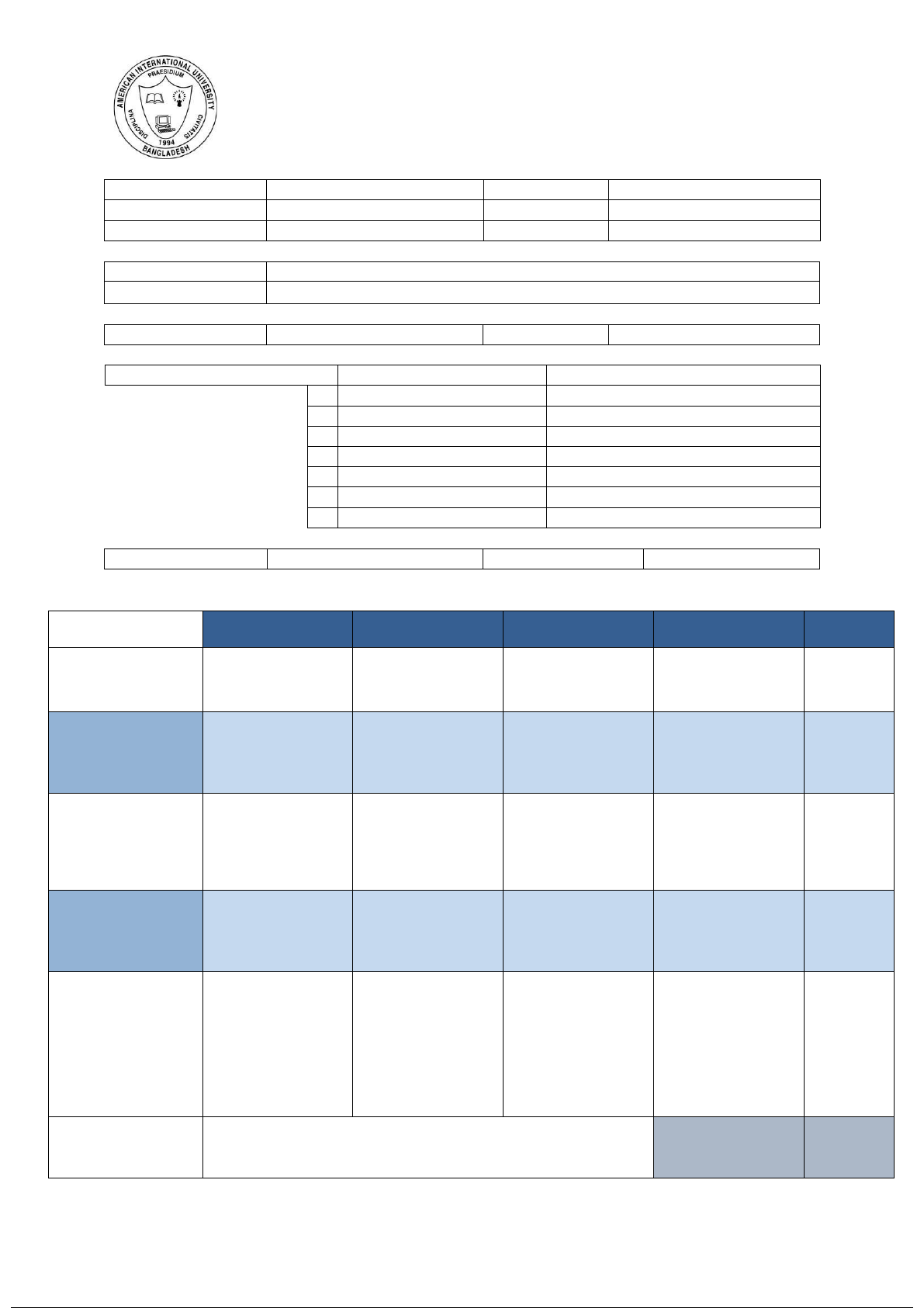
elaborated and

connected; effective transitions between sentences; no typographic, spelling, or grammatical errors.

effective transitions between sentences; minor typographic, spelling, or grammatical errors.

some lack of clarity, typographic, spelling, or grammatical errors are present.

Very unclear, many errors.

Comments: Total Marks

(Out of ):



# Abstract :

This experiment explores the construction and characterization of MOSFET logic gates. Through systematic assembly and analysis, the functionality and performance of basic logic gates, such as AND, OR, and NOT are investigated. The study aims to enhance understanding of MOSFET-based digital circuit design and its applications in modern electronics.

# Problem statement :

The problem statement for this experiment revolves around the construction and analysis of MOSFET logi gates. Despite the widespread use of MOSFETs in digital circuits, students often lack hands-on experienc their practical implementation and performance evaluation. This experiment aims to address this gap by providing a structured approach to building MOSFET-based logic gates, including AND, OR, and NOT gat Key challenges include understanding the behavior of MOSFETs in different configurations, ensuring prop biasing and connection schemes, and analyzing the gate characteristics and transfer characteristics. Addi issues related to voltage levels, signal integrity, and noise immunity need to be considered for reliable ope By investigating these aspects, the experiment aims to enhance students' understanding of MOSFET-bas logic design principles and prepare them for practical applications in fields such as integrated circuit desig microelectronics, and digital systems engineering.

# Aim & Objective:

The aim of this experiment is to:

* To construct MOSFET-based logic gates including AND, OR, and NOT gates.
* To understand the behavior and characteristics of MOSFETs in different configurations.
* To explore proper biasing techniques for MOSFET logic gates.
* To analyze the gate characteristics and transfer characteristics of the constructed logic gates.
* To investigate the voltage levels, signal integrity, and noise immunity considerations for reliable operation.
* To enhance understanding of MOSFET-based digital logic design principles.
* To prepare students for practical applications in integrated circuit design, microelectronics, and digit systems engineering.

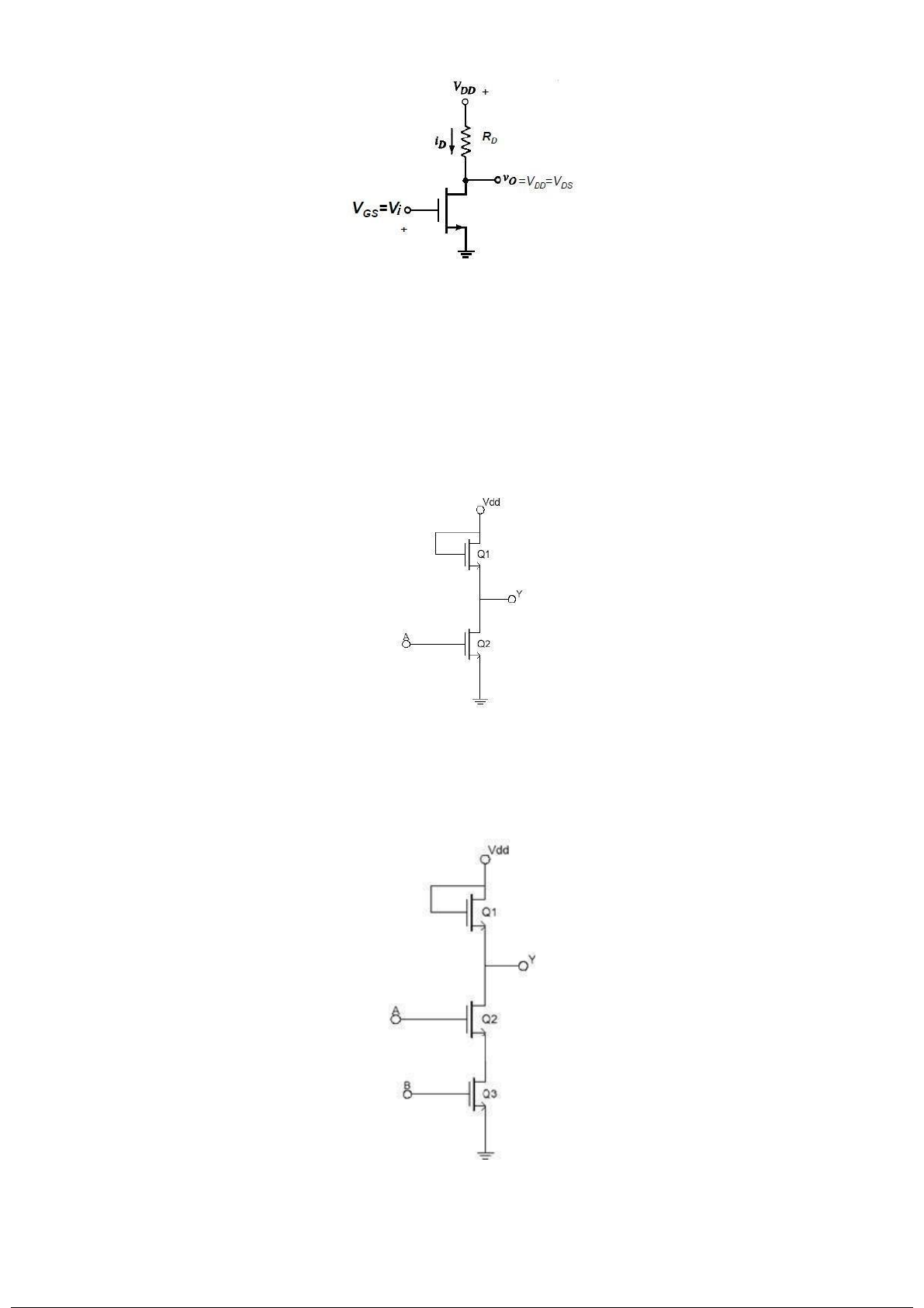
# Theory :

NMOS Inverter with Ohmic/ Resistive Load:

Considering an ideal scenario, when a HIGH (+5V) is applied to the input, the NMOS transistor turns ON a current flows from Vdd to ground; thus output voltage, Vo= 0V.

Similarly, if a LOW (0V) is applied to the input, the NMOS remains in its OFF state. As a result, the current from Vdd has no path to ground. The output voltage is +5V

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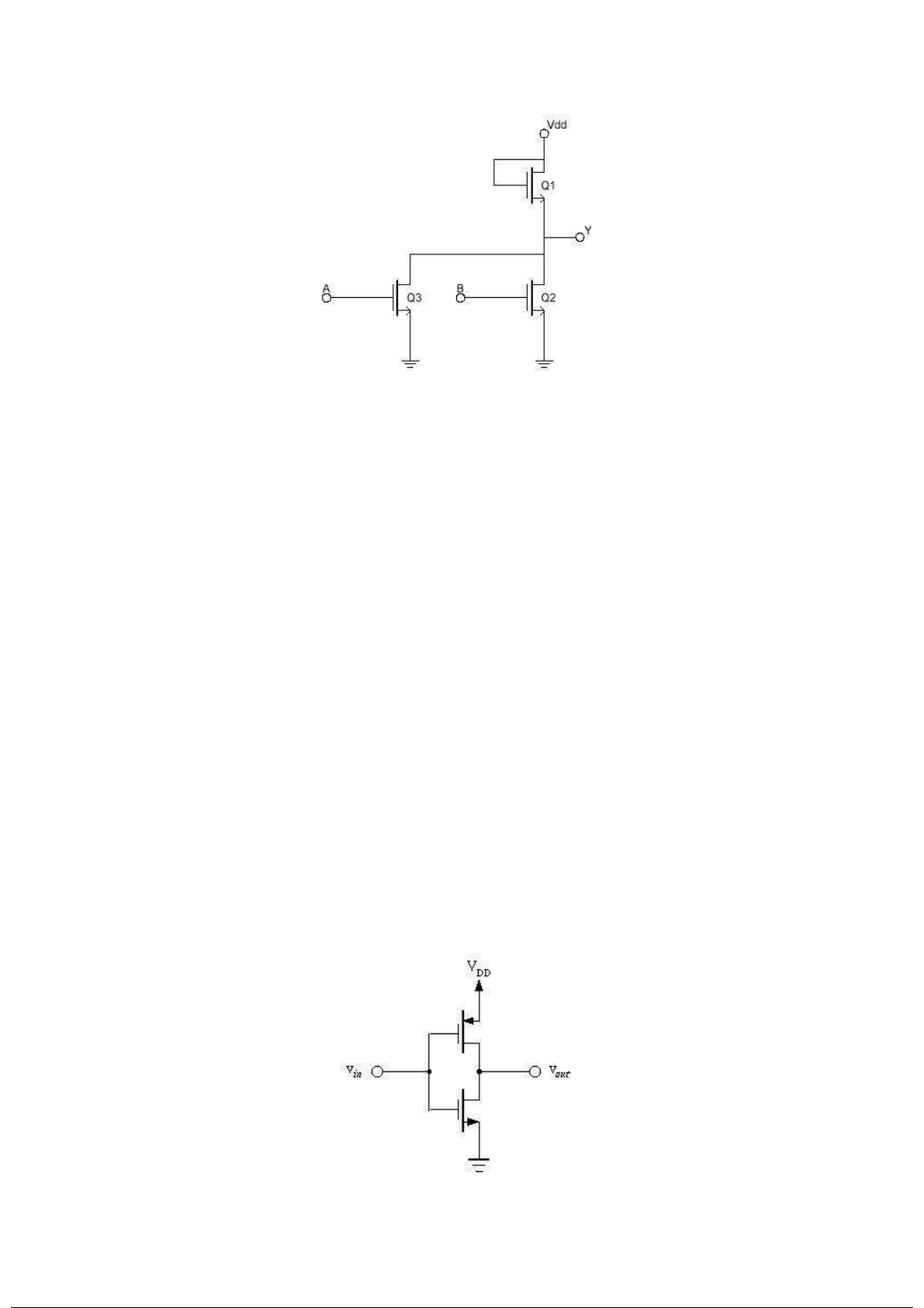
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NMOS NOR Gate:

Figure 4 : NMOS NOR Gate

**CMOS Logic:**

CMOS transistors are smaller in size and provide less power dissipation than NMOS transistors. Thus they became the obvious choice of replacing NMOS transistors at the integrating circuit level design in all applications.

CMOS consists of one p-channel MOSFET or PMOS and one NMOS. The two MOSFETs are designed to have matching characteristics. Thus, they are complementary to each other. When OFF, their

resistance is effectively infinite; when ON, their channel resistance is quite low (around 200 Ω). Since the gate is essentially an open circuit it draws no current and the output voltage will be equal to either ground or to the power supply voltage, depending on which transistor is conducting.

CMOS Inverter:

When the input is grounded (logic 0), the N-channel MOSFET is unbiased, and therefore has no channel enhanced within itself. It is an open circuit, and therefore leaves the output line disconnected from ground. At the same time, the P-channel MOSFET is forward biased, so it has a channel enhanced within itself.

This channel has a resistance of about 200 Ω, connecting the output line to the +V supply. This pulls the

output up to +V (logic 1).

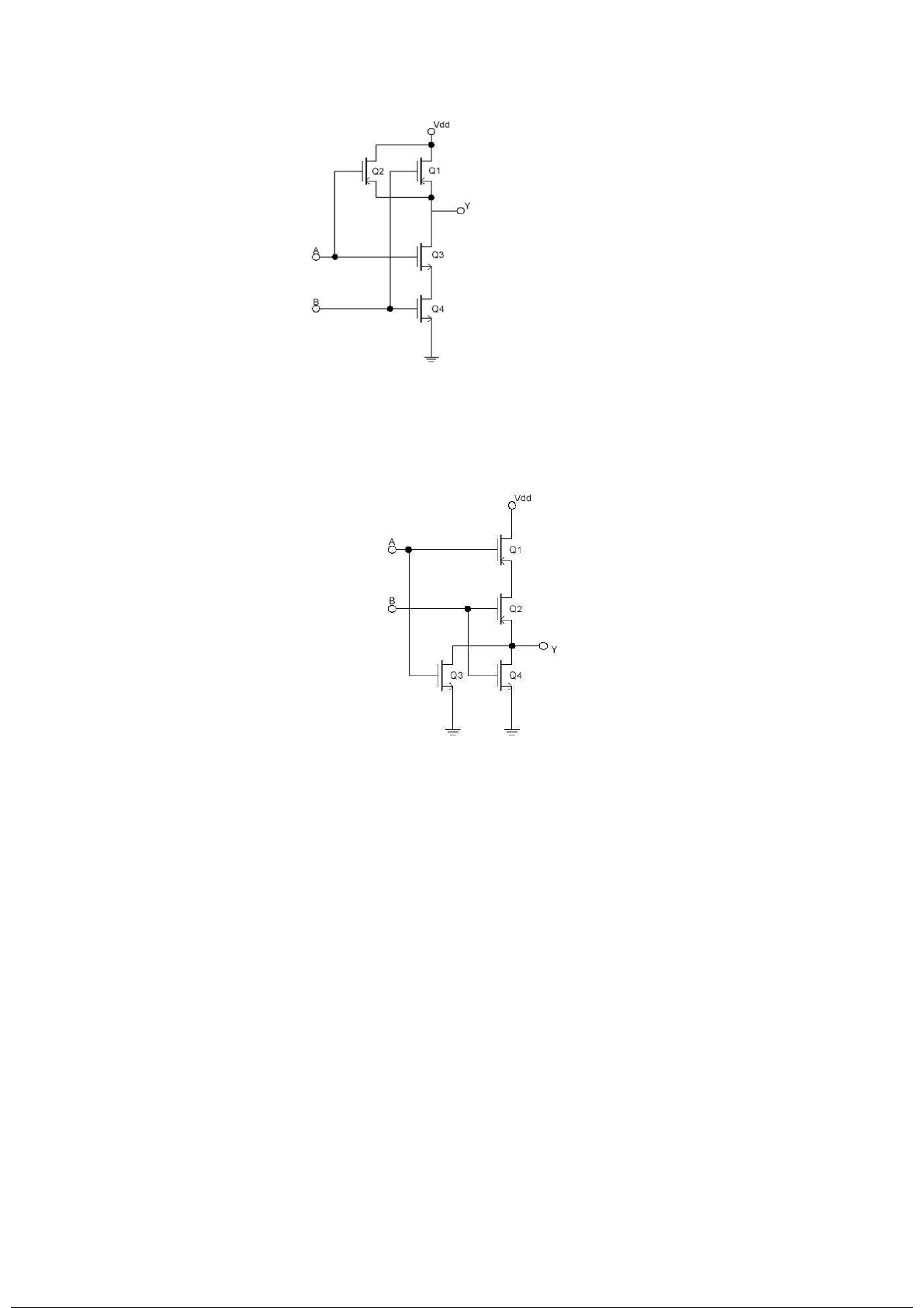
When input A is at +V (logic 1), the P-channel MOSFET is off and the N-channel MOSFET is on, thus pulling the output down to ground (logic 0). Thus, this circuit correctly performs logic inversion, and at the same time provides active pull-up and pull-down, according to the output state.

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**CMOS NAND Gate:**

Figure 5 : CMOS Inverter

Figure 6 : CMOS NAND Gate



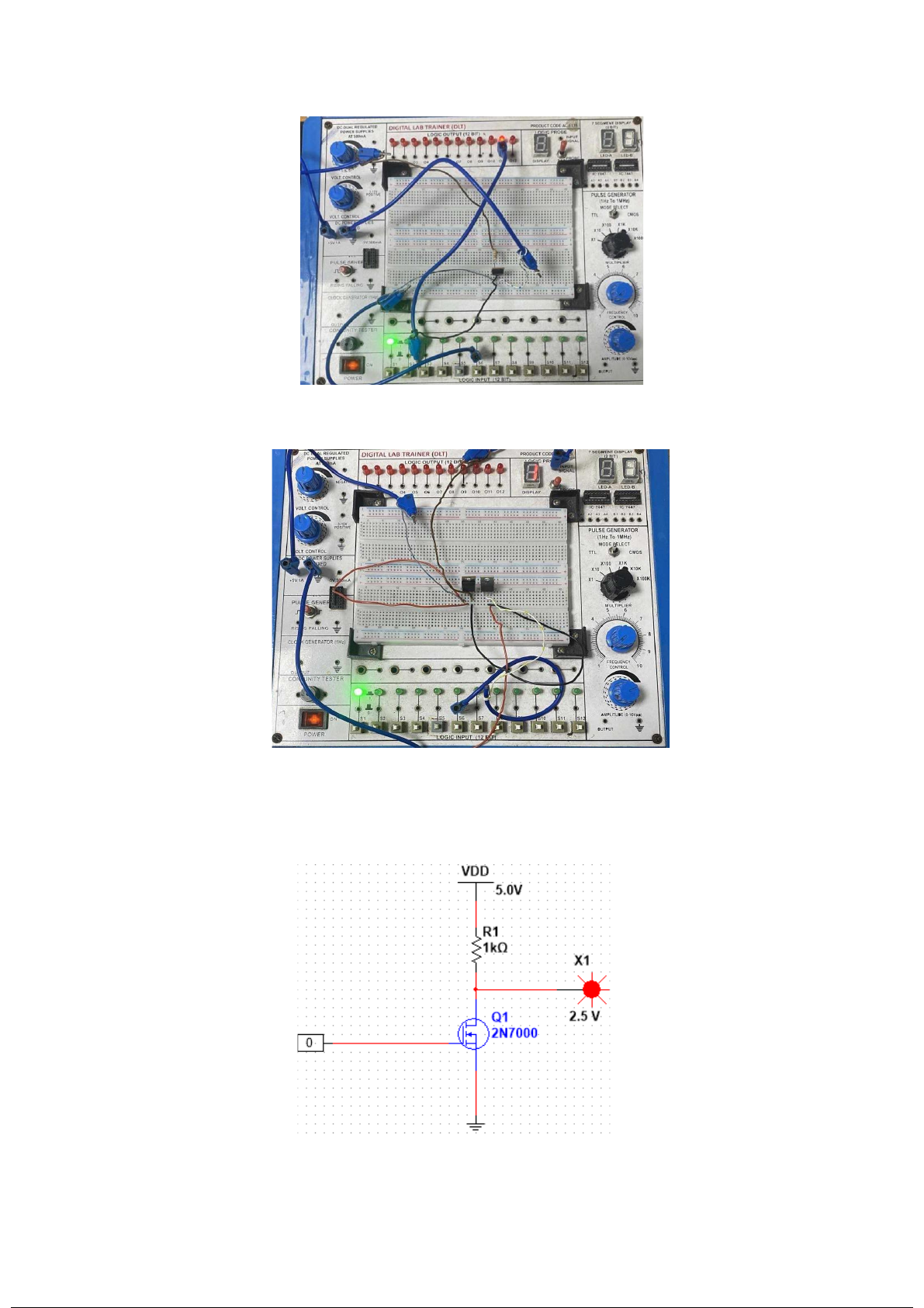
**CMOS NOR Gate:**

Figure 7 : CMOS NOR Gate

# List of components :

* 10KΩ resistor (brown-black-orange).
* 1N914 diodes or equivalent.
* Connecting wires.
* Trainer Board

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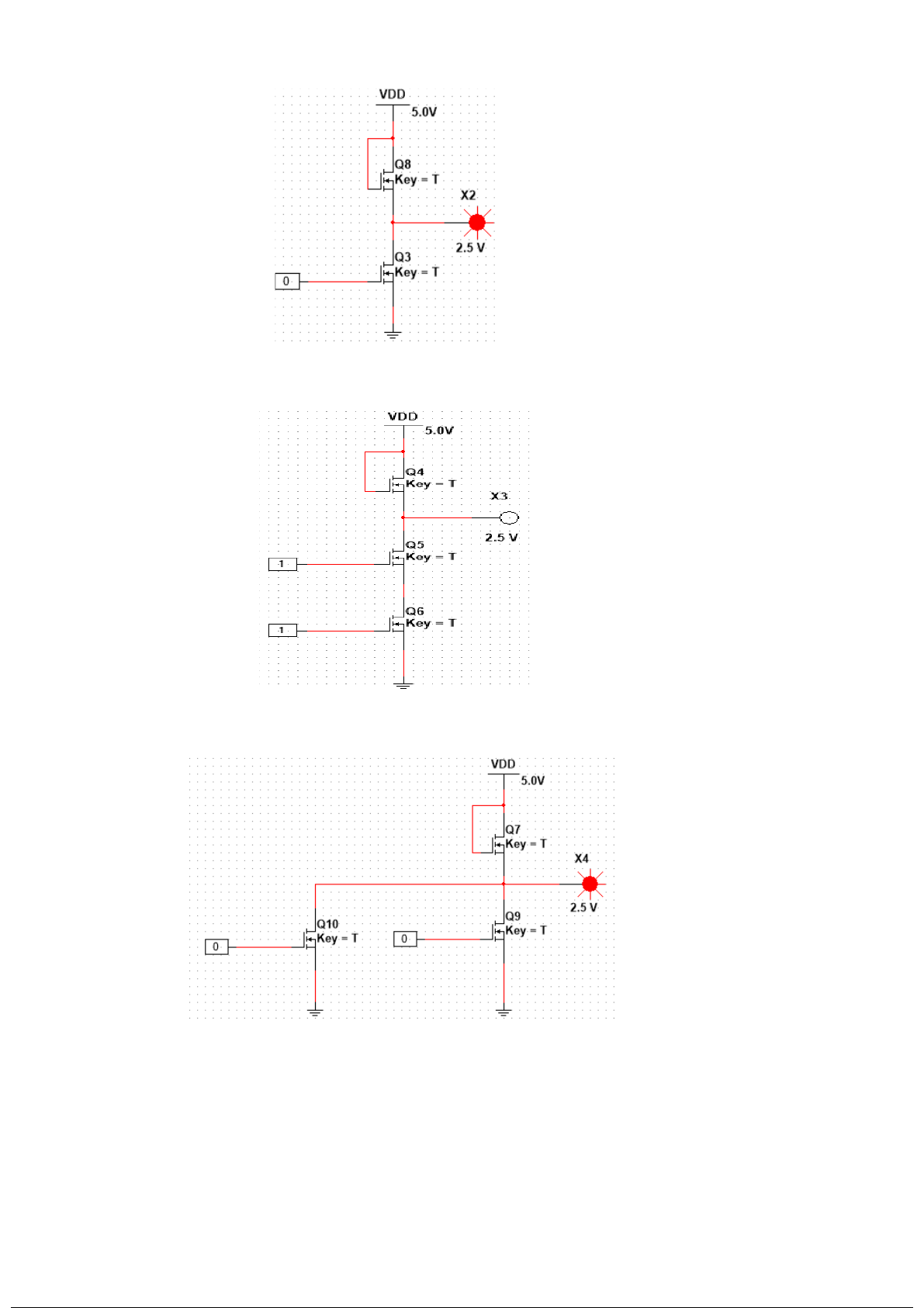


Figure 11 : NMOS Inverter with NMOS Load

Figure 12 : NMOS NAND Gate

Figure 13 : NMOS NOR Gate

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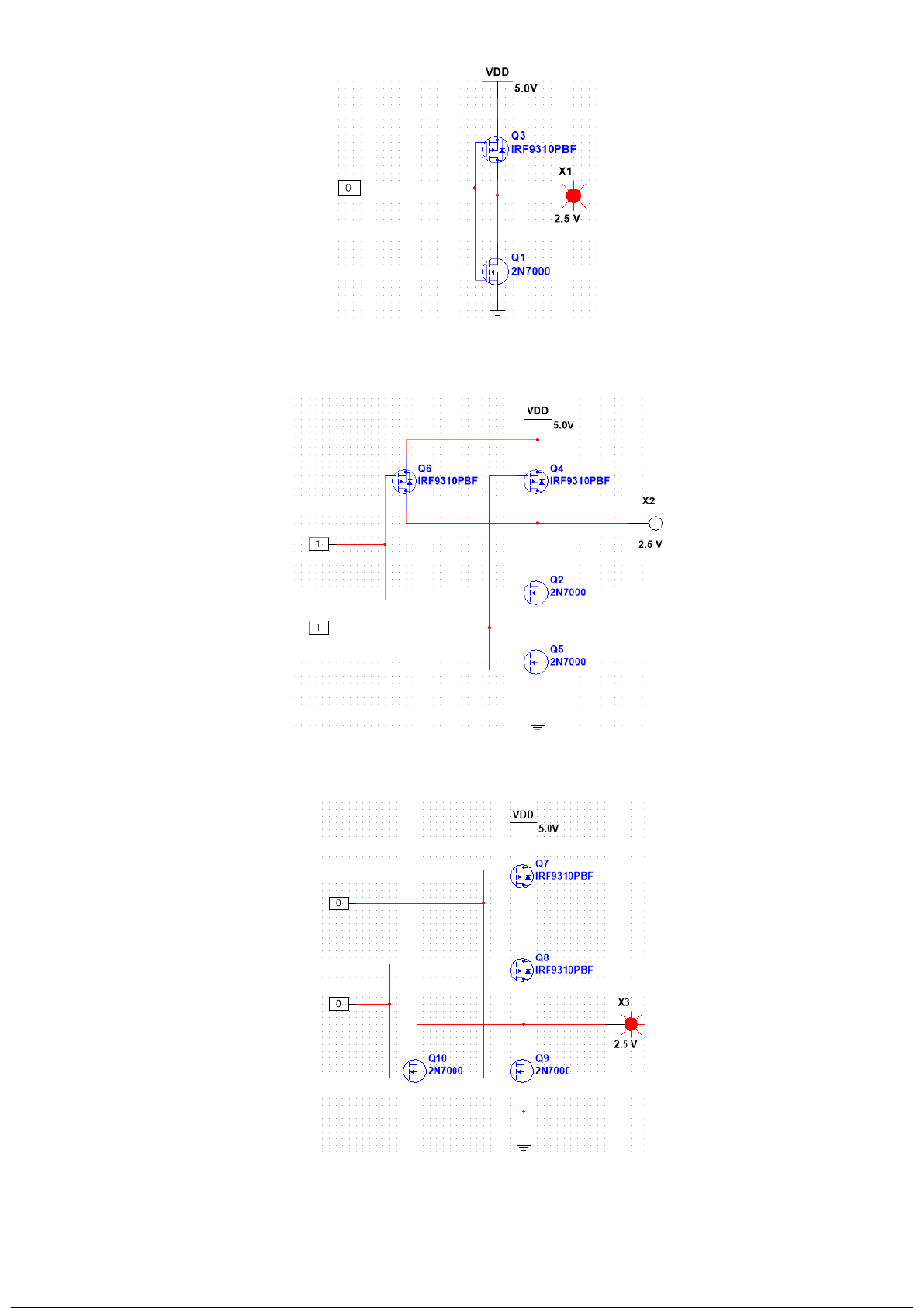


Figure 14 : CMOS Inverter

Figure 15 : CMOS NAND Gate

Figure 16 : CMOS NOR Gate

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